

54AC378

54AC378 Parallel D Register with Enable



Literature Number: SNOS143

54AC378 Parallel D Register with Enable

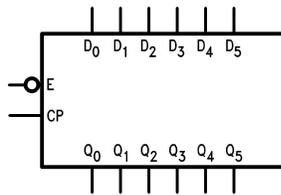
General Description

The AC378 is a 6-bit register with a buffered common Enable. This device is similar to the AC174, but with common Enable rather than common Master Reset.

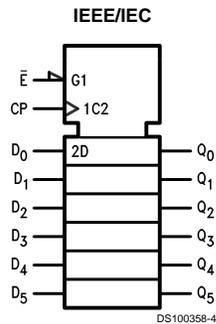
Features

- 6-bit high-speed parallel register
- Positive edge-triggered D-type inputs
- Fully buffered common clock and enable inputs
- Input clamp diodes limit high-speed termination effects
- Standard Microcircuit Drawing (SMD) 5962-9160501

Logic Symbols



DS100358-1



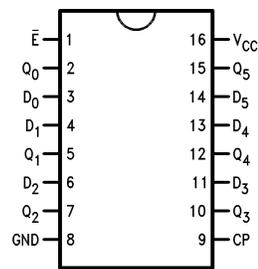
DS100358-4

Pin Descriptions

Pin Names	Description
\bar{E}	Enable Input (Active LOW)
D ₀ -D ₅	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
Q ₀ -Q ₅	Outputs

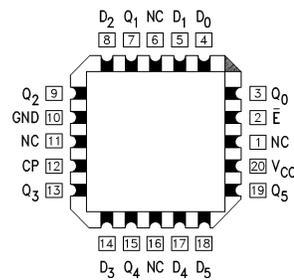
Connection Diagrams

Pin Assignment for DIP and CERPACK



DS100358-2

Pin Assignment for LCC



DS100358-3

Functional Description

The AC378 consists of six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable (\bar{E}) inputs are common to all flip-flops.

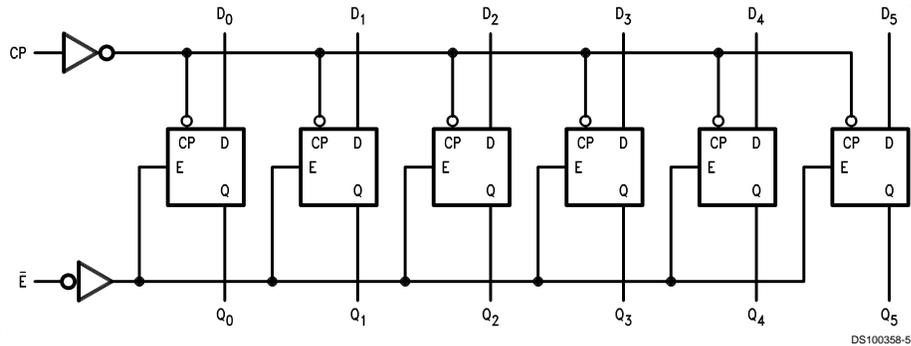
When the \bar{E} input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the \bar{E} input is HIGH the register will retain the present data independent of the CP input.

Truth Table

Inputs			Output
\bar{E}	CP	D_n	Q_n
H	N	X	No Change
L	N	H	H
L	N	L	L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 N = LOW-to-HIGH Clock Transition

Logic Diagram



DS100358-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	± 50 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Junction Temperature (T_J)	

CDIP

175°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
AC	2.0V to 6.0V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	-55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Characteristics for AC Family Devices

Symbol	Parameter	V_{CC} (V)	$T_A = -55^\circ\text{C to } +125^\circ\text{C}$		Units	Conditions
			Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	2.1		V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	3.15			
		5.5	3.85			
V_{IL}	Maximum Low Level Input Voltage	3.0	0.9		V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	1.35			
		5.5	1.65			
V_{OH}	Minimum High Level Output Voltage	3.0	2.9		V	$I_{OUT} = -50 \mu A$
		4.5	4.4			
		5.5	5.4			
		3.0	2.4		V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -12$ mA $I_{OH} = -24$ mA $I_{OH} = -24$ mA (Note 2)
		4.5	3.7			
	5.5	4.7				
V_{OL}	Maximum Low Level Output Voltage	3.0	0.1		V	$I_{OUT} = 50 \mu A$
		4.5	0.1			
		5.5	0.1			
		3.0	0.4		V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 12$ mA $I_{OL} = 24$ mA $I_{OL} = 24$ mA
		4.5	0.5			
	5.5	0.5				
I_{IN}	Maximum Input Leakage Current	5.5	± 1.0		μA	$V_I = V_{CC}, GND$
I_{OLD}	Minimum Dynamic Output Current (Note 3)	5.5	50		mA	$V_{OLD} = 1.65V$ Max
I_{OHD}		5.5	-50		mA	$V_{OHD} = 3.85V$ Min
I_{CC}	Maximum Quiescent Supply Current	5.5	80.0		μA	$V_{IN} = V_{CC}$ or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V) (Note 4)	T _A = -55°C to +125°C C _L = 50 pF		Units
			Min	Max	
f _{max}	Maximum Clock Frequency	3.3	95		MHz
		5.0	95		
t _{PLH}	Propagation Delay CP to Q _n	3.3	1.5	12.0	ns
		5.0	1.5	9.0	
t _{PHL}	Propagation Delay CP to Q _n	3.3	1.5	12.0	ns
		5.0	1.5	9.0	

Note 4: Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

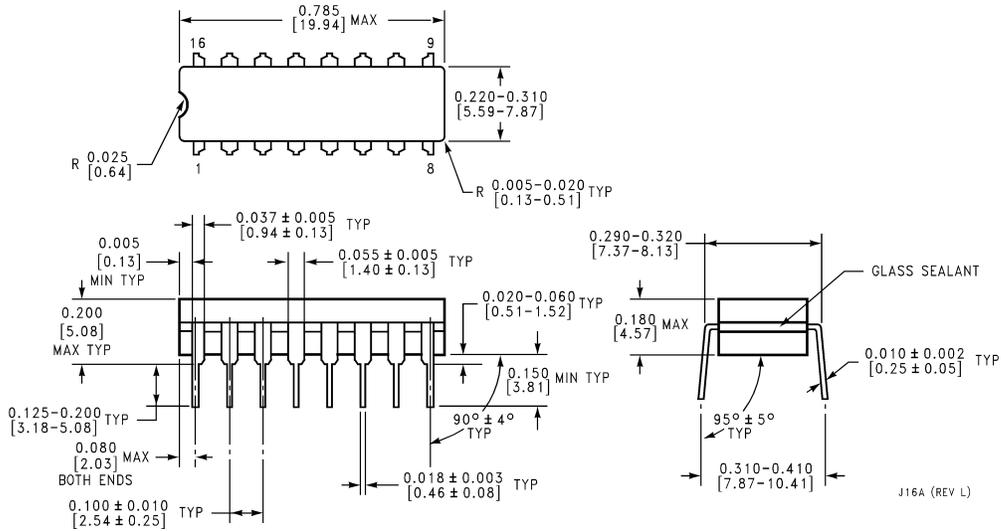
Symbol	Parameter	V _{CC} (V) (Note 5)	T _A = -55°C to +125°C C _L = 50 pF	Units
			Guaranteed Minimum	
t _s	Setup Time, HIGH or LOW D _n to CP	3.3	4.0	ns
		5.0	4.0	
t _h	Hold Time, HIGH or LOW D _n to CP	3.3	4.0	ns
		5.0	4.0	
t _s	Setup Time, HIGH or LOW, \bar{E} to CP	3.3	2.5	ns
		5.0	2.5	
t _h	Hold Time, HIGH or LOW, \bar{E} to CP	3.3	4.0	ns
		5.0	4.0	
t _w	CP Pulse Width HIGH or LOW	3.3	6.5	ns
		5.0	6.5	

Note 5: Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

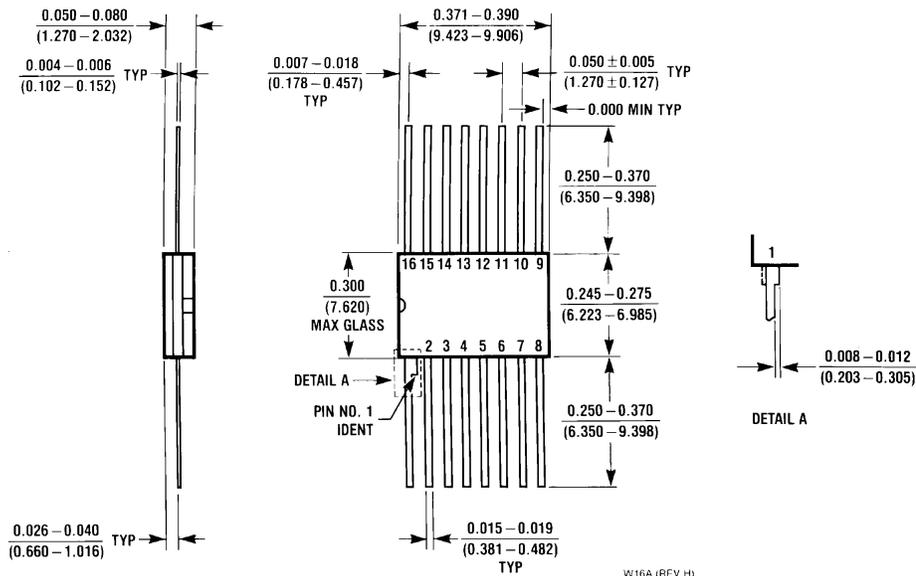
Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	28	pF	V _{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted



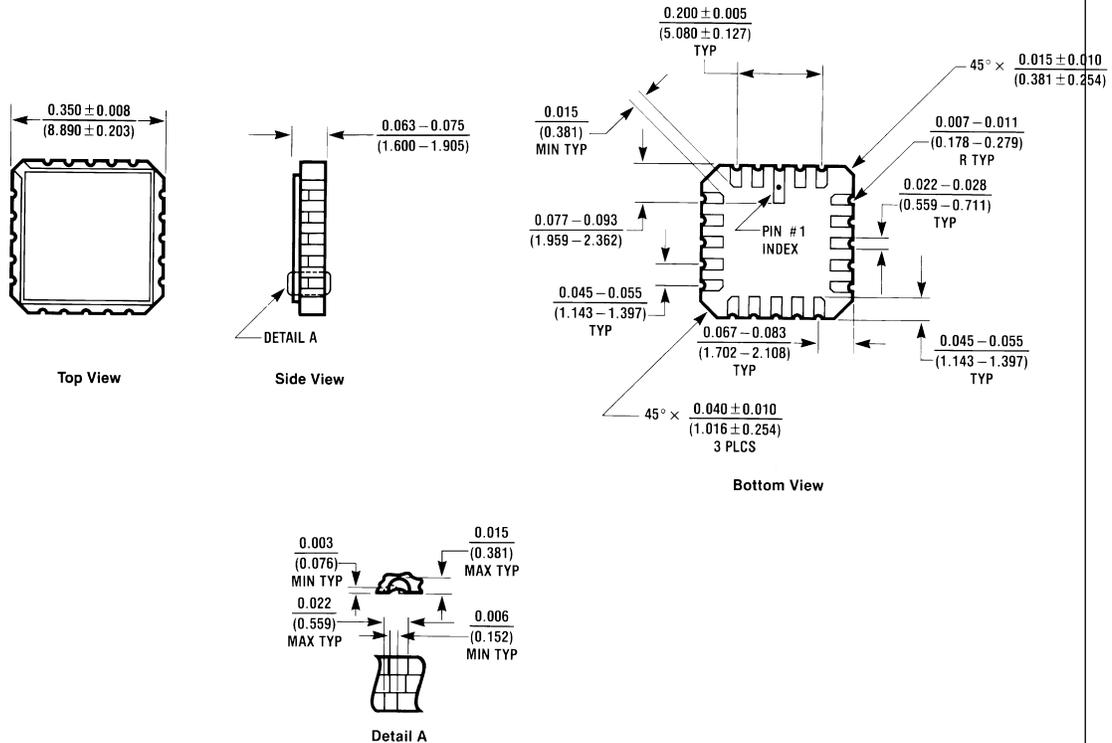
**16-Lead Ceramic Dual-in-line
Package Number J16A**



**16-Lead CERPACK
Package Number W16A**

54AC378 Parallel D Register with Enable

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Ceramic Leadless Chip Carrier
Package Number E20A**

E20A (REV. D)

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