ADVANCE INFORMATION



74LVT16373

3.3V ABT 16-Bit Transparent Latch with TRI-STATE® Outputs

General Description

The LVT16373 contains sixteen non-inverting latches with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is low, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the outputs are in high Z state.

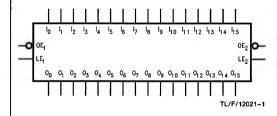
These latches are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16373 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V VCC
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16373
- Latch-up performance exceeds 500 mA

Ordering Code: See Section 11

Logic Symbol



Pin Names	Description	
ŌĒn	Output Enable Input (Active Low)	
LEn	Latch Enable Input	
I ₀ -I ₁₅	Inputs	
O ₀ -O ₁₅	TRI-STATE Outputs	

	SSOP	TSSOP JEDEC
Order Number		74LVT16373MTD 74LVT16373MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for

$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	SSOP and TSSOP				
O0 - 2 47 - 10 O1 - 3 46 - 11 GND - 4 45 - GND O2 - 5 44 - 12 O3 - 6 43 - 13 VCC - 7 42 - VCC O4 - 8 41 - 14 O5 - 9 40 - 15 GND - 10 39 - GND O6 - 11 38 - 16 O7 - 12 37 - 17 O8 - 13 36 - 18 O9 - 14 35 - 19 GND - 15 34 - GND O1 - 16 33 - 110 O1 - 17 32 - 11 VCC - 18 31 - VCC O1 - 19 30 - 112 O1 - 20 29 - 113 GND - 21 28 - GND O1 - 21 28 - GND O1 - 22 27 - 114 O1 - 22 27 - 114 O1 - 23 26 - 115	_				
O1 — 3	0E ₁ —	1	48	- LE ₁	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	0₀ —	2	47	— 1 ₀	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	01	3	46	— I _I	
03 6 43 -13 V _{CC} 7 42 -V _{CC} 04 8 41 -14 05 9 40 -15 GND 10 39 -GND 06 11 38 -16 07 12 37 -17 08 13 36 -18 09 14 35 -19 GND 15 34 -GND 01 16 33 -10 01 17 32 -11 V _{CC} 18 31 -V _{CC} 01 19 30 -12 01 21 28 -GND 01 22 -13 -14 01 22 -14 -14 01 10 10 -15 -16 01 10 17 32 -11 01 10 10 -10 -10 01 10 10 -10 -10	GND —	4	45	— GND	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	02 -	5	44	— I ₂	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	03 -	6	43	— I ₃	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$		7	42	– v _{cc}	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	04	8	41	— I₄	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	05 -	9	40	— I ₅	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	GND -	10	39	— GND	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	o ₆ —	11	38	— I ₆	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	07 —	12	37	- I ₇	
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	o ₈ —	13	36	— I ₈	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	o ₉ —	14	35	— I ₉	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	GND —	15	34	— GND	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	o ₁₀ —	16	33	- I ₁₀	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	011	17	32	-111	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	v _{cc} —	18	31	— v _{cc}	
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	012	19	30	- 1 ₁₂	
$0_{14} - 22$ 27 -1_{14} $0_{15} - 23$ 26 -1_{15}		20	29	— I ₁₃	
0 ₁₅ — 23 26 — 1 ₁₅	GND -	21	28	— GND	
$ \begin{array}{ccccccccccccccccccccccccccccccccc$	014 -	22	27	ا ا ₁₄	
\overline{OE}_2 — 24 25 — LE_2	015	23	26		
	0E ₂ —	24	25	— LE ₂	

TL/F/12021-2

Functional Description

The LVT16373 contains sixteen D-type latches with TRI-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable (LEn) input is HIGH, data on the Dn enters the latches. In this condition the latches are transparent, i.e., a latch output will change states each time its D input changes. When LEn is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LEn. The TRI-STATE standard outputs are controlled by the Output Enable (OEn) input. When OEn is LOW, the standard outputs are in the 2-state mode. When OEn is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Tables

Inputs			Outputs
LE ₁	ŌE ₁	10-17	00-07
Х	н	Х	z
Н	L	L	L
Н	L	н	н
L	L	X	00

Inputs			Outputs
LE ₂	ŌE ₂	I ₈ -I ₁₅	O ₈ -O ₁₅
Х	Н	X	Z
Н	L	L	⊕ L
Н	L	Н	н
L	L	X	00

H = High Voltage Level

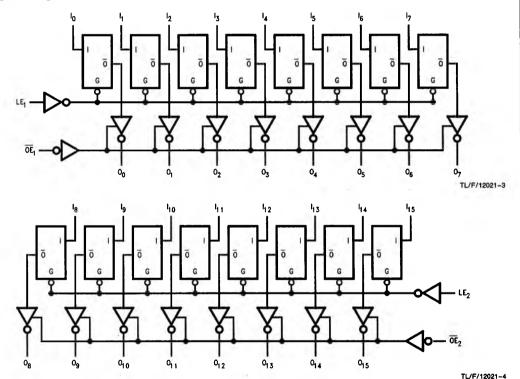
L = Low Voltage Level

X = Immaterial

Z = High Impedance

O_o = Previous output prior to HIGH to LOW transition of LE

Logic Diagrams



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.