National Semiconductor

74LVX174
Low Voltage Hex D Flip-Flop with Master Reset

General Description

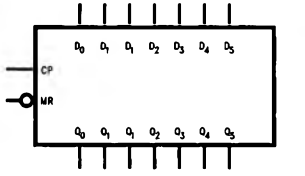
The LVX174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Ordering Code: See Section 11

Logic Symbols



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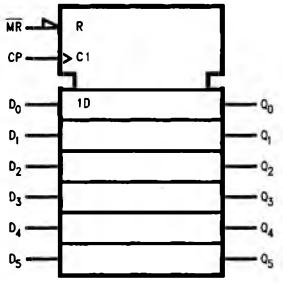
IEEE/IEC



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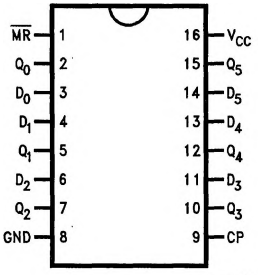
Connection Diagram

Pin Assignment for SOIC and SSOP



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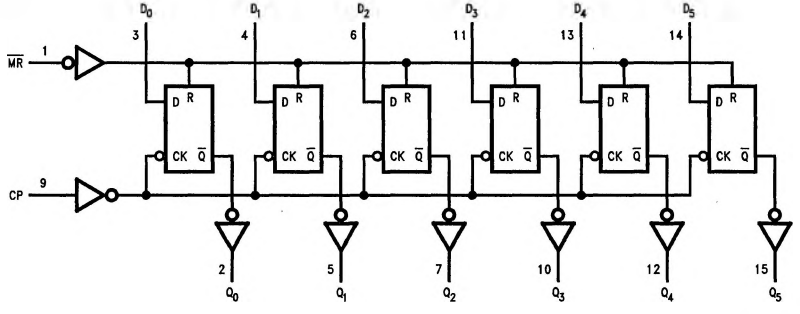
Logic Diagram



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Pin Names	Description
D_0–D_5	Data Inputs
CP	Clock Pulse Input
$\overline{MR}$	Master Reset Input
Q_0–Q_5	Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX174M 74LVX174MX	74LVX174SJ 74LVX174SJX	74LVX174MSCX
See NS Package Number	M16A	M16D	MSC16

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	180 mW

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time ($\Delta t/\Delta v$)	0 ns/V to 100 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	74LVX174 T_A = +25°C			74LVX174 T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V		
V_{IL}	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V		
V_{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V_{IN} = V_{IL} or V_{IH}	I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −4 mA
V_{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V	V_{IN} = V_{IL} or V_{IH}	I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX174 T_A = 25°C		Units	C_L (pF)
			Typ	Limit		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.3	0.5	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.3	−0.5	V	50
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: (Input $t_r = t_f = 3$ ns)

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX174 T_A = +25°C			74LVX174 T_A = −40°C to +85°C		Units	C_L (pF)
			Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Time CP to Q_n	2.7		7.6	14.5	1.0	17.5	ns	15
				10.1	18.0	1.0	21.0		50
		3.3 ±0.3		5.9	9.3	1.0	11.0		15
				8.4	12.8	1.0	14.5		50
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	2.7		7.9	15.0	1.0	18.5	ns	15
				10.4	18.5	1.0	22.0		50
		3.3 ±0.3		6.2	9.7	1.0	11.5		15
				8.7	13.2	1.0	15.0		50
t_S	Setup Time D_n to CP	2.7	7.5			8.5		ns	
		3.3 ±0.3	5.0			6.0			
t_H	Hold Time D_n to CP	2.7	0			0			
		3.3 ±0.3	0			0			
t_{REM}	Removal Time $\overline{MR}$ to CP	2.7	4.5			4.5		ns	
		3.3 ±0.3	3.0			3.0			
t_W	Clock Pulse Width	2.7	6.5			7.5			
		3.3 ±0.3	5.0			5.0			
t_W	$\overline{MR}$ Pulse Width	2.7	6.5			7.5		ns	
		3.3 ±0.3	5.0			5.0			
f_{MAX}	Maximum Clock Frequency	2.7	65	130		55		MHz	15
			45	60		40			50
		3.3 ±0.3	115	180		95			15
			65	95		55			50
t_{OSLH} t_{OSHL}	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	50

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

Symbol	Parameter	74LVX174 T_A = +25°C			74LVX174 T_A = −40°C to +85°C		Units
		Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 1)		29				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{4 \text{ (per F/F)}}$